CLAIMS

What is claimed is:

1. A method of generating a physical netlist for an integrated circuit design including steps of:

(a) receiving as input a representation of a core cell for a hierarchical integrated circuit design;

(b) generating a physical netlist for a core cell model tile that maps logical ports of the core cell to physical ports of the core cell model tile;

(c) including values for parasitic resistances connecting the logical ports of the core cell to the physical ports of the core cell model tile in the physical netlist for the core cell model tile;

(d) connecting a hierarchical array of core cell model tiles so that the physical ports of each core cell model tile are connected to one another inside the array or mapped to an input/output port of the hierarchical array of core cell model tiles; and

(e) generating as output a physical netlist of the hierarchical array of core cell model tiles.

2. The method of Claim 1 wherein step (c) further comprises including values for parasitic inductances connecting the logical ports of the core cell to the physical ports of the core cell model tile in the physical netlist for the core cell model tile.

3. The method of Claim 1 wherein step (c) further comprises including values for parasitic capacitances of the core cell in the physical netlist for the core cell model tile.

4. The method of Claim 1 further comprising a step (f) of simulating the integrated circuit design from the physical netlist.

5. The method of Claim 4 further comprising a step (g) of performing a timing analysis of the integrated circuit design from the physical netlist.

6. A computer program product for generating a physical netlist for an integrated circuit design comprising:

a medium for embodying a computer program for input to a computer; and

a computer program embodied in the medium for causing the computer to perform steps of:

(a) receiving as input a representation of a core cell for a hierarchical integrated circuit design;

(b) generating a physical netlist for a core cell model tile that maps logical ports of the core cell to physical ports of the core cell model tile;

(c) including values for parasitic resistances connecting the logical ports of the core cell to the physical ports of the core cell model tile in the physical netlist for the core cell model tile;

(d) connecting a hierarchical array of core cell model tiles so that the physical ports of each core cell model tile are connected to one another inside the array or mapped to an input/output port of the hierarchical array of core cell model tiles; and

(e) generating as output a physical netlist of the hierarchical array of core cell model tiles.

7. The computer program product of Claim 6 wherein step (c) further comprises including values for parasitic inductances connecting the logical ports of the core cell to the physical ports of the core cell model tile in the physical netlist for the core cell model tile.

8. The computer program product of Claim 6 wherein step (c) further comprises including values for parasitic capacitances of the core cell in the physical netlist for the core cell model tile.

9. The computer program product of Claim 6 further comprising a step (f) of simulating the integrated circuit design from the physical netlist.

10. The computer program product of Claim 9 further comprising a step (g) of performing a timing analysis of the integrated circuit design from the physical netlist.